
Plan-IQ 2.5.1.3 Download

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Field of the Invention The present invention relates generally to a semiconductor memory circuit, and more particularly to a semiconductor memory circuit for storing an address signal being applied through an input circuit in response to an address signal applied to an address terminal of the memory circuit through a decoder. 2. Description of the Background Art Referring to FIG. 3, a background-art semiconductor memory circuit includes a memory array 5 consisting of a plurality of memory cells for storing data, a row decoder 1 comprising a plurality of word decoders 1-1 to 1-n each of which is turned on to decode a row address signal AX applied through an address terminal (not shown) and to select a corresponding word line based on the decoded row address signal AX to thus select a memory cell connected to the selected word line, and a column decoder 2 which is responsive to a column address signal CA applied through an address terminal to select a corresponding bit line of the memory array 5 to thereby apply a signal on the selected bit line to a corresponding sense amplifier. Referring to FIGS. 1 and 2, the word decoder 1-1 shown in FIG. 2 includes a MOS transistor 1a turned on to select the word line WL connected to the memory array 5 according to the row address signal AX applied through the address terminal, an N-channel MOS transistor 1b responsive to the signal of the MOS transistor 1a to render a drain of the MOS transistor 1a conductive and a second gate electrode of the MOS transistor 1a nonconductive, and an inverter 1c responsive to the MOS transistor 1b to apply an output from the inverter 1c to a first gate electrode of the MOS transistor 1a. The row decoder 1 further includes a NAND circuit 1d responsive to the output of the inverter 1c to apply an output signal from the NAND circuit 1d to the second gate electrode of the MOS transistor 1a. The inverter 1c receives the output of the

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