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A: It is a server issue, try another time. Or you can try to contact the support team directly. 1. Field of the Invention The present invention generally relates to a semiconductor memory device and a method of operating the same, and more particularly to a semiconductor memory device including a voltage down converter that provides a constant internal supply voltage when the external power supply voltage is less than a target level, and a method of operating the same. 2. Description of the Related Art An operational voltage range is not necessarily in correspondence with the external voltage range applied to a semiconductor memory device, but includes a wide range of voltage values ranging from a ground voltage to a supply voltage level. A semiconductor memory device typically includes a voltage down converter that generates a constant internal supply voltage to be applied to internal circuit devices in accordance with the external voltage range applied thereto. FIG. 1A is a block diagram illustrating a conventional semiconductor memory device including a voltage down converter. Referring to FIG. 1A, the conventional semiconductor memory device includes a voltage down converter 11, an internal power supply control unit 12, a buffer circuit 13, an input/output circuit 14, and an input/output pad PAD. The voltage down converter 11 receives an external power supply voltage VPin externally applied, and generates a constant internal supply voltage VIN corresponding thereto. An output voltage VOUT of the constant internal supply voltage VIN is input to the input/output circuit 14, and the buffer circuit 13. The internal power supply control unit 12 receives the output voltage VOUT. FIG. 1B is a circuit diagram illustrating the buffer circuit 13 illustrated in FIG. 1A. Referring to FIG. 1B, the buffer circuit 13 includes a PMOS transistor M1 having a source connected to a constant voltage generator VCCG and a gate connected to the internal power supply control unit 12, and an NMOS transistor M2 having a source connected to the constant voltage generator VCCG and a drain connected to an output node OUT. The operation of the buffer circuit 13 will now be described. When the output voltage VOUT

of the voltage down converter 11 is low, the constant voltage generator VCCG is turned on to thereby apply a high voltage to the output node OUT, so that the PMOS transistor M1 and the NMOS transistor M2 are turned on, so that the output voltage VOUT is increased. On the contrary, when the output voltage VOUT of 6d1f23a050

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